Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **5**
2. **1**
3. **0**
4. **2**
5. **6**
6. **7**
7. **3**
8. **VSS**
9. **8**
10. **4**
11. **9**
12. **CARRY OUT**
13. **CLOCK INHIBIT**
14. **CLOCK**
15. **RESET**
16. **VDD**

**.095”**

**.081”**

**15 14 13 12 11**

**10**

**9**

**8**

**16**

**1**

**2**

**3 4 5 6 7**

**MASK**

**REF**

**C**

**D**

**4**

**0**

**1**

**7**

**B**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4017B**

**APPROVED BY: DK DIE SIZE .081” X .095” DATE: 2/4/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .024” P/N: CD4017BH**

**DG 10.1.2**

#### Rev B, 7/1